

Figure P3.10

Since gate voltage is high, the midpoint V_x is expected to be low. Therefore, the lead is in saturation and the driver is in linear region. From KCL

$$\frac{1}{2}k \cdot \frac{W}{L} + V \cdot V \cdot (V)^2 \cdot \frac{1}{2}k \cdot \frac{W}{2} \cdot 2 + V \cdot V \cdot V^2$$

Using the following two equations to iterate find the solution.

$$V_{T,L}(V_s) = 0.48 \text{ } 0.52$$
 $V_{T,L}(V_s) = 0.48 \text{ } 0.52$ $V_{T,L}(V_s) = 0.48 \text{ } 0.52$

The intermediate values are listed in the table:

$V_{T,L}(V_n) = [$	V _n
0.480	0.1523
0.518	0.1337
0.513	-0.1359
0.514	0.1357
0.514	0.1357

$$I_D = \frac{1}{2} \frac{W}{L} (1.04V , V^2) = 0.516810 1.04 0.1357 0.1357^2 = 103.1[A]$$

3.11 The following parameters are given for an nMOS process:

$$r_{sr}=16 \text{ Å}$$

substrate doping $N_s=4\cdot10^{19}\,\mathrm{cm^3}$
polysilicon gate doping $N_o=2\cdot10^{19}\,\mathrm{cm^3}$
oxide-interface fixed-charge density $N_{sr}=2\cdot10^{19}\,\mathrm{cm^3}$

- (a) Calculate V_f for an unimplanted transistor.
- (b) What type and what concentration of impurities must be implanted to achieve $V_p=+0.6~{\rm V}$ and $V_p=-0.6~{\rm V}$?

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