No.	Scoring Indicators										Split score	Total score					
					РД	RT-/	۸.			-							1
1 1	There are four segment register in 8086																
	Code segment register (CS)												2				
	Data segment register (DS)														1		
	Extra segment register (ES)														1		
	Stack segment register (SS)																
2	The way in which a source operand is denoted in an instruction is known												2				
	as addressing mode.											1 5 5	5x2=10				
	Assem	daller et	Bre-ctil	we list	a moves	Chicken II	o the	mercus.	colhlair	that i	resille de	Property	to tro	me forte	500		
3	Assembler directive is a message to the assembler that tells it how to translate instructions into machine code.												2				
4	100000000000000000000000000000000000000															-	
	Real address mode ,protected virtual address mode and virtual 8086 mode.  Core is the processor within the CPU.												2				
5	Corre is	time p	modes	SOF W	erthan i	the C	PU.							1	-	2	51
						= -	PART	-B				500	C .	+			
							V6000030					100					
01.1	Single +5V power supply																
	2. Clock speed range of 5-10MHz																
	<ol> <li>capable of executing about 0.33 MIPS (Millions instructions per second)</li> <li>It is 16-bit processor having 16-bit ALU, 16-bit registers, internal data bus,</li> </ol>																
	and 16-bit external data bus resulting in faster processing.												6	10000			
	<ol><li>It uses two stages of pipelining, i.e. Fetch Stage and Execute Stage, which</li></ol>													1000000	6		
	improves performance.																
	<ol><li>Fetch stage can prefetch up to 6 bytes of instructions and stores them in the queue.</li></ol>																
	7.				niumbs.	129	Carren	Sec. 1									
	7. It has 256 interrupts. (any five)																
					- 2.5	Section 1											
					100000		400	- 6	7	- 6	- 55	4	3	2	1.		
2	15	1-4	13	12	10	10	1	T		1							
2	15 X	14 ×	13 X	12 X	0	D	1	т	s	z	×	Ac	×	P	×		
2	×	X Over	or story for	X	No.		ī	т	s	z		Ac	×	P	х		
2	×	X Over	X rflow fi	x lag	No.		ì	Т	s	z		Ac	×	P	×		
2	X	X Over	X rflow fi ction fi rupt fil	x lag	No.		ī	Т	S	z		Ac	×	P	×		
2	X D T	X Over Dire Inter Trap Sign	X rflow fi ction fi rupt fi flag	x lag	No.		1	T	S	Z		Ac	×	P	×	6	
2	X O D I T S	X Over Director Inter Trap Sign Zero	X rilow fi ction fi rupt fi flag flag	lag lag lag	O		ī	т	S	z		Ac	×	Р	×	6	6
2	X D I I T S Z	X Over Directory Inter Trap Sign Zero Auxi	X rflow fi ction fi rupt fi flag flag flag flag	lag lag lag ag	O		ī	т	S	z		Ac	×	P	×	6	6
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