

$$C_{GSD} = C_{GDD} = C_{ox} \cdot L_D = 1.73 \times 10^{-7} \times 0.2 \times 10^{-4} \\ = 3.46 \times 10^{-12} [F/cm] = 3.46 \times 10^{-12} [F/m]$$

Thus, the SPICE input file is as follows:

```

M1 6 12 4 7 NMOS W=5U L=30U LD=0.20 AS=34P PS=24.4U AD=93P
+ PD=42.4U
.MODEL NMOS NMOS (VTO=0.85 KP=45U LAMDA=0.05 GAMMA=0.32
+ PHI=0.615 PB=0.837 CJS=1.41E-4 CJSW=3.2E-10
+ CGSO=3.46E-10 CGDO=3.46E-10 NS=0.33 NDSW=0.5)

```

- 4.2 A layout of nMOS transistors in NAND2 gate is shown below. Write a SPICE description corresponding to the layout. The diffusion region between two polysilicon gates can be split equally between the two transistors.

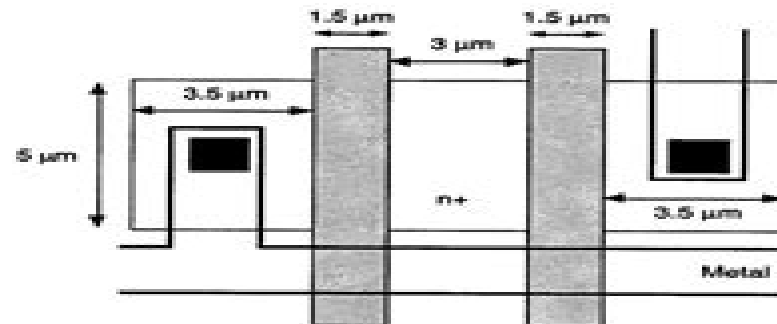


Figure P4.2

**SOLUTION:**

The SPICE input list could be as follows:

```

M1 2 1 0 0 NMOS W=5U L=1.5U AS=17.5P AD=7.5P PS=17U PD=8U
M2 4 3 2 0 NMOS W=5U L=1.5U AS=7.5P AD=17.5P PS=8U PD=17U

```

- 4.3 Using the SPICE LEVEL 1 MOSFET model equations, derive an expression for the sensitivity of the drain current  $I_D$  with respect to temperature. Calculate the sensitivity at room temperature  $T=300K$  by using the values in Example 4.1. For simplicity, assume that  $n_i$  is independent of temperature. Also verify your solution numerically by calculating  $I_D$  at 310K and then  $\Delta I_D/\Delta T$ .

**SOLUTION:**

The sensitivity of drain current with respect to temperature  $T$  can be expressed by:

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**Sung-Mo Kang, Yusuf Leblebici**



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