Reg. No.:	

Question Paper Code: 40989

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024

Fifth Semester

Electronics and Communication Engineering

EC 3552 - VLSI AND CHIP DESIGN

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2021)

Time: Three hours

Maximum: 100 marks

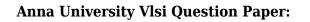
Answer ALL questions.

PART A — $(10 \times 2 = 20 \text{ marks})$

- How NMOS and PMOS act as a switch?
- What is the body effect of MOS transistor?
- 3. Draw the stick diagram for two input NOR gate.
- 4. What is the significance of propagation delay?
- Differentiate latches and flipflops.
- 6. What are the basic timing classifications of digital systems?
- List the interconnect parameters in chip design.
- Write the logic equation for 4-bit comparators.
- 9. Sketch the ASIC design flow?
- Differentiate embedded cores and SOCs.

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JL Elias



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