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web as an alternative you can also write your simulation stimulus using generic vhd code called a testbench the testbench codes gets compiled along with the design so that the stimulus is also in the compiled simulation model ieee came along and created additional libraries that are supported by almost all vhd compilers specific silicon

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web for sample syntax and a list of vhd statements supported by the vhd synthesizer see appendix a quick reference for a list of exceptions and constraints on the vhd synthesizer s support of vhd see appendix b limitations this chapter shows you the structure of a vhd design and then

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to describe the input and output ports of this circuit 1 entity circuit 1 is 2 port a in std logic 3 b in std logic 4 out1 out std logic 5 end circuit 1

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