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Question Paper Code : 40989

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024

Fifth Semester

Electronics and Communication Engineering

EC 3552 – VLSI AND CHIP DESIGN

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How NMOS and PMOS act as a switch?
2. What is the body effect of MOS transistor?
3. Draw the stick diagram for two input NOR gate.
4. What is the significance of propagation delay?
5. Differentiate latches and flipflops.
6. What are the basic timing classifications of digital systems?
7. List the interconnect parameters in chip design.
8. Write the logic equation for 4-bit comparators.
9. Sketch the ASIC design flow?
10. Differentiate embedded cores and SOC's.

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Emilie Sanchez



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