



Figure P3.10

Since gate voltage is high, the midpoint V_x is expected to be low. Therefore, the load is in saturation and the driver is in linear region. From KCL

$$I_D = I_{D,driver} = I_{D,load}$$

$$\frac{1}{2} k' \frac{W}{L} (1 V - V_x)^2 = \frac{1}{2} k' \frac{W'}{L'} (2.1 V - V_x)^2$$

Using the following two equations to iterate find the solution.

$$V_{T,d}(V_x) = 0.48 - 0.52 \sqrt{1.01 V_x} = \sqrt{1.01} V_x$$

The intermediate values are listed in the table:

$V_{T,d}(V_x)$	V_x
0.480	0.1523
0.518	0.1337
0.513	0.1359
0.514	0.1357
0.514	0.1357

$$I_D = \frac{1}{2} k' \frac{W}{L} (1.04 V - V_x)^2 = 0.516810 (1.04 - 0.1357)^2 = 103.1 [\text{A}]$$

3.11 The following parameters are given for an nMOS process:

$$t_{ox} = 16 \text{ \AA}$$

$$\text{substrate doping } N_a = 4 \cdot 10^{15} \text{ cm}^{-3}$$

$$\text{polysilicon gate doping } N_p = 2 \cdot 10^{19} \text{ cm}^{-3}$$

$$\text{oxide-interface fixed-charge density } N_{ox} = 2 \cdot 10^{11} \text{ cm}^{-2}$$

(a) Calculate V_T for an unimplanted transistor.

(b) What type and what concentration of impurities must be implanted to achieve $V_{T,p} = +0.6 \text{ V}$ and $V_{T,n} = -0.6 \text{ V}$?

Analysis And Design Of Digital Integrated Circuits Solution Manual

Marco Cascella



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