

# Scan and ATPG Process Guide (DFTAdvisor™, FastScan™ and FlexTest™)

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# **And Atpg Process Guide**

**Wai-Kai Chen** 

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Sun, Saman Kiamehr, 2019-09-12 This book provides readers with a detailed reference regarding two of the most important long term reliability and aging effects on nanometer integrated systems electromigrations EM for interconnect and biased temperature instability BTI for CMOS devices The authors discuss in detail recent developments in the modeling analysis and optimization of the reliability effects from EM and BTI induced failures at the circuit architecture and system levels of abstraction Readers will benefit from a focus on topics such as recently developed physics based EM modeling EM modeling for multi segment wires new EM aware power grid analysis and system level EM induced reliability optimization and management techniques Reviews classic Electromigration EM models as well as existing EM failure models and discusses the limitations of those models Introduces a dynamic EM model to address transient stress evolution in which wires are stressed under time varying current flows and the EM recovery effects Also includes new parameterized equivalent DC current based EM models to address the recovery and transient effects Presents a cross layer approach to transistor aging modeling analysis and mitigation spanning multiple abstraction levels Equips readers for EM induced dynamic reliability management and energy or lifetime optimization techniques for many core dark silicon microprocessors embedded systems lower power Nanometer Technology Designs Nisar Ahmed, 2010-02-26 Adopting new many core processors and datacenters fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects With design size in millions of gates and working frequency in GHz timing related defects have become a high proportion of the total chip defects For nanometer technology designs the stuck at fault test alone cannot ensure a high quality level of chips At speed tests using the transition fault model has become a requirement in technologies below 180nm Traditional at speed test methods cannot guarantee high quality test results as they face many new challenges Supply noise including IR drop ground bounce and Ldi dt effects on chip performance high test pattern volume low fault defect coverage small delay defect test pattern generation high cost of test implementation and application and utilizing low cost testers are among these challenges This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test Memory, Microprocessor, and ASIC Wai-Kai Chen, 2003-03-26 Timing memory power dissipation testing and testability are all crucial elements of VLSI circuit design In this volume culled from the popular VLSI Handbook experts from around the world provide in depth discussions on these and related topics Stacked gate embedded and flash memory all receive detailed treatment including their power cons

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