Qп. No.	Scoring Indicators												Split score	Total			
					PA	RT-	Δ.										
1 2	There are four segment register in 8086														1		
		- Table 1					200									2	1
	Code segment register (CS) Data segment register (DS)														1		
	Extra segment register (ES)													1.0			
	Stack segment register (SS)																
2	The way in which a source operand is denoted in an instruction is known												2				
	as addressing mode.											150	5×2=10				
3	Assembler directive is a message to the assembler that tells it how to translate																
	instru															2	
4	Real a	ddres	s mod	le ,pr	otecte	d virt	ual ac	idres	s mod	le and	wirtu	al 808	6 mo	down		2	
5	Cone is														h.,	2	1 61
							PART	D.				5.5	-	-			1.00
								100				(7)					
					er sup						1		7				
1.1	Clock speed range of 5-10MHz																
	 capable of executing about 0.33 MIPS (Millions instructions per second) It is 16-bit processor having 16-bit ALU, 16-bit registers, internal data bus, 																
		amd	16-bit	so to the	rnal da	eta bi	es ness	ultimo	in the	COURT OF	Right care	s, Imrue	rriar c	sata D	us,	G	1
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	It uses two stages of pipelining, i.e. Fetch Stage and Execute Stage, which improves performance.														100		
	6. Fetch stage can prefetch up to 6 bytes of instructions and stores them in																
	the queue.																
	7. it has 256 interrupts. (any five)																
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2	15	14	13	12	13	10	9	8	7	6	5	4	3	2	1		
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	D — Direction flag																
	I — Interrupt flag T — Trap flag																
	S — Sign flag													6	6		
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