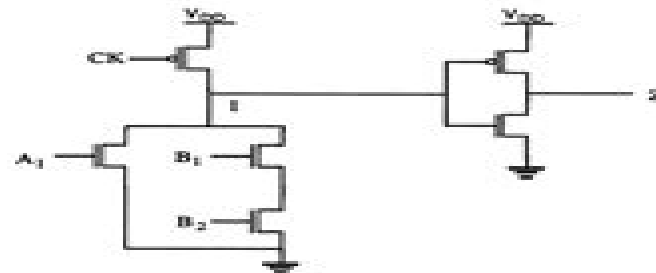


$$\begin{aligned}
 V_{CK} &= 5\text{V}, & t < 0 \\
 V_{CK} &= 0\text{V}, & 0 \leq t < T_w \\
 V_{CK} &= 5\text{V}, & t \geq T_w \\
 V_{DD} &= 5\text{V}
 \end{aligned}$$

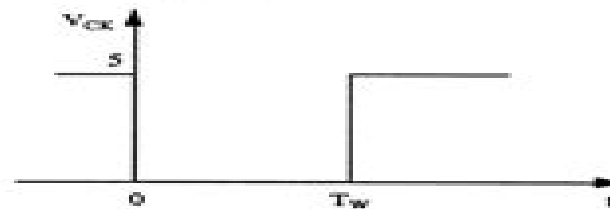
- v) At $t = 0$, the node voltage at I is zero.
vi) The input voltages at A_1 , B_1 and B_2 are zero for $0 \leq t \leq T_w$. Find the minimum T_w that allows V_I to reach 2.5 V.

SOLUTION:

(a). The circuit diagram is drawn below:



(b). When the clock signal changes from high to low and A_1 , B_1 , and B_2 are low, node I is charged from 0 to 2.5V through the pMOS transistor.



The transistor first operates in saturation region and then in linear region. Thus,

$$T_w = t_{sat} + t_{lin}$$

When $0 < V_I < 1\text{V}$, the transistor is saturated.

$$I = -C \frac{dV_I}{dt}$$

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